LSISAS1064 4-Port 3 Gbit/s Serial Attached SCSI Controller

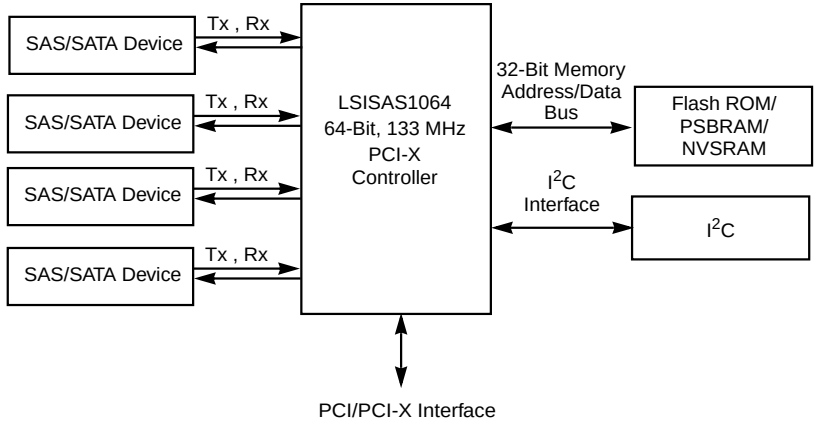
Datasheet

Version 2.0

The LSISAS1064 is a 4-port, 3.0 Gbit/s SAS/SATA controller that is compliant with the Fusion-MPT™ architecture, provides a PCI-X interface, and supports Integrated RAID™.

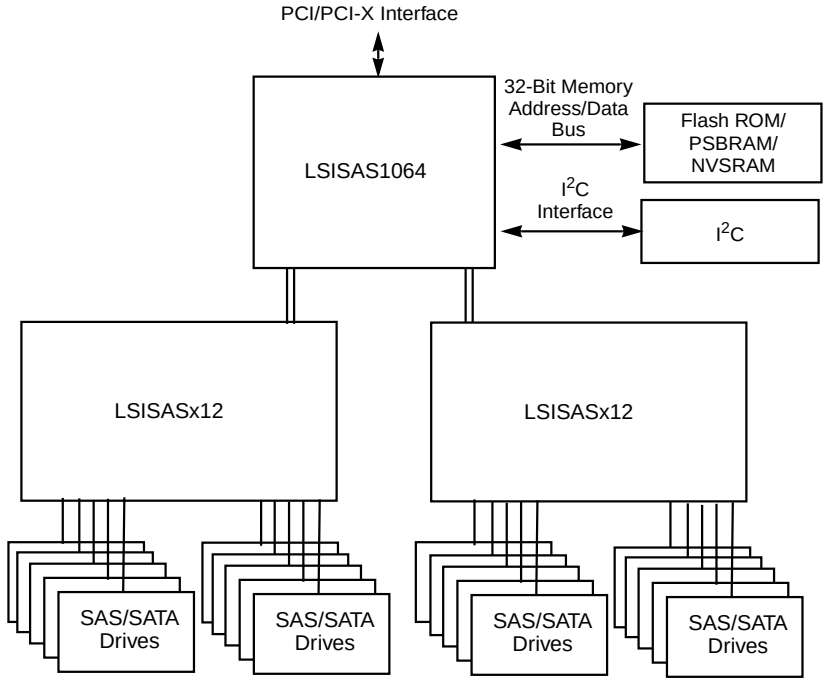
The LSISAS1064 controller brings 3.0 Gbit/s SAS performance to host adapter, workstation, and server designs, making it easy to add a SAS interface to any PCI or PCI-X[1] system. The LSISAS1064 integrates four high-performance SAS/SATA phys and a 64-bit, 133 MHz PCI-X bus master DMA core. Each of the four phys on the LSISAS1064 is capable of 3.0 Gbit/s and 1.5 Gbit/s SAS link rates and 3.0 Gbit/s and 1.5 Gbit/s SATA link rates. The LSISAS1064 supports the ANSI *Serial Attached SCSI Standard,* Version 1.0. The controller also supports the Serial ATA (SATA) protocol defined by the *Serial ATA Specification,* Version 1.0a. Supporting both the SAS and SATA interfaces, the LSISAS1064 is a versatile controller that provides the backbone of both server and high-end workstation environments. Figure 1 shows a direct-connect configuration. Figure 2 provides an example of the LSISAS1064 configured with an LSISASx12 expander.

Figure 1 LSISAS1064 Direct-Connect Example Application



1. In some instances, this manual references PCI-X explicitly. References to the PCI bus may be inclusive of both the PCI specification and PCI-X addendum, or may only refer to the PCI bus depending on the operating mode of the device.

Figure 2 LSISAS1064 Controller and LSISASx12 Expander Example Application



The SAS interface uses the proven SCSI data transfer command set to ensure reliable data transfers while providing the connectivity and flexibility of point-to-point serial data transfers. The SAS interface provides improved performance, simplified cabling, smaller connectors, lower pin count, and lower power requirements when compared to parallel SCSI. SAS controllers leverage an electrical and physical connection interface that is compatible with Serial ATA technology.

Each port on the LSISAS1064 supports SAS and SATA devices using the SAS Serial SCSI Protocol (SSP), Serial Management Protocol (SMP), Serial Tunneling Protocol (STP), and SATA. The SSP enables communication with other SAS devices. SATA enables the LSISAS1064 to communicate with other SATA devices. The SMP communicates topology management information directly with an attached SAS expander device, such as the LSISASx12. STP enables the LSISAS1064 to communicate with a SATA device through an attached expander.

The LSISAS1064 supports a 133 MHz, 64-bit PCI-X bus. With the exception that the PCI interface is not tolerant of 5 V PCI, the interface

is backward compatible with all revisions of the PCI/PCI-X bus. The LSISAS1064 supports PCI-X split completion cycles and 32-bit or 64-bit data bursts with variable burst length. The LSISAS1064 supports the *PCI-X Addendum to the PCI Local Bus Specification,* Revision 2.0, and the *PCI Local Buss Specification,* Revision 3.0.

The LSISAS1064 supports the Integrated RAID solution, which is a highly integrated, low-cost RAID implementation. It is designed for systems requiring redundancy and high availability but not needing a full-featured RAID implementation. The Integrated RAID solution includes Integrated Mirroring™ (IM) technology and Integrated Striping™ (IS) technology. IM provides physical mirroring of up to eight physical drives. IM requires a nonvolatile RAM (NVSRAM) to support write journaling. IS enables data striping across up to eight physical drives. The Integrated RAID solution is OS-independent, easy to install and configure, and does not require a special driver. The runtime operation of the Integrated RAID solution is transparent to the operating system. A single firmware build supports all Integrated RAID capabilities. The LSISAS1064 also provides Zero Channel RAID (ZCR) support.

The LSISAS1064 is based on the Fusion-MPT (Message Passing Technology) architecture, which features a performance-based message passing protocol that offloads the host CPU by completely managing all I/Os and minimizes system bus overhead by coalescing interrupts. The Fusion-MPT architecture requires only a thin, easy to develop device driver that is independent of the I/O bus. LSI Logic provides this device driver.

To meet its flexibility and data transfer requirements, the LSISAS1064 uses an ARM®926 processor. The ARM926 offers data cache and instruction cache, which provide a significant performance increase.

LSI Logic manufactures the LSISAS1064 controller using the Gflx™ technology.

Features

This section provides a summary of the LSISAS1064 features and benefits.

SAS Features

SAS features include:

- Provides four fully independent phys
- Supports 3.0 Gbit/s and 1.5 Gbit/s SAS data transfers for each phy
- Supports SSP to enable communication with other SAS devices
- Supports SMP to communicate topology management information
- Provides a serial, point-to-point, enterprise-level storage interface
- Simplifies cabling between devices
- Provides a scalable interface that supports up to 128 devices through multiple expanders
- Supports wide ports consisting of two, three, or four phys
- Supports narrow ports consisting of a single phy
- Transfers data using SCSI information units

SATA and STP Features

SATA and STP features include:

- Supports SATA data transfers of 3.0 Gbits/s and 1.5 Gbits/s
- Supports STP data transfers of 3.0 Gbits/s and 1.5 Gbits/s
- Provides a serial, point-to-point storage interface
- Simplifies cabling between devices
- Eliminates the Master-Slave construction used in parallel ATA
- Allows addressing of multiple SATA targets through an expander
- Allows multiple initiators to address a single target (in a fail-over configuration) through an expander

PCI Performance

PCI features of the LSISAS1064 include:

- Supports a 133 MHz, 64-bit PCI/PCI-X interface that does the following:
  - Operates up to 133 MHz PCI-X
  - Operates at 33 MHz or 66 MHz PCI
  - Supports 32-bit or 64-bit data transfers
  - Supports 32-bit or 64-bit addressing through Dual Address Cycles (DAC)
  - Provides a theoretical 1066 Mbytes/s PCI bandwidth
  - Supports 3.3 V PCI, and is not 5 V PCI tolerant
  - Complies with the *PCI Local Bus Specification*, Revision 3.0
  - Complies with the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 2.0
  - Complies with the *PCI Power Management Interface Specification*, Revision 1.2
  - Complies with the *PC2001 Specification*
- Provides unequaled performance through the Fusion-MPT architecture
- Provides high throughput and low CPU utilization to offload the host processor
- Uses a dedicated ARM926 processor
- Presents a single electrical load to the PCI bus
- Reduces Interrupt Service Routine (ISR) overhead with interrupt coalescing
- Supports Message Signaled Interrupts (MSI) and MSI-X
- Supports 32-bit or 64-bit data bursts with variable burst lengths
- Supports the PCI Cache Line Size register
- Supports the PCI Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple commands

- Supports the PCI-X Memory Read Dword, Split Completion, Memory Read Block, and Memory Write Block commands
- Supports up to 16 PCI-X Split Transaction cycles

Integration

These features make the LSISAS1064 easy to integrate:

- Supports backward compatibility with previous revisions of the PCI specification, with the exception that the LSISAS1064 does not support 5 V PCI
- Provides a full 32-bit or 64-bit PCI-X DMA bus master
- Reduces time-to-market with the Fusion-MPT architecture that provides:
  - Single driver binary for SAS/SATA, SCSI, and Fibre Channel products
  - One firmware build that supports all Integrated RAID capabilities
  - Thin and easy-to-develop drivers
  - Reduced integration and certification effort

Usability

The usability features include:

- Simplifies cabling with point-to-point, serial architecture
- Smaller, thinner cables do not restrict airflow
- Provides drive spin-up sequencing control
- Provides up to two LED signals for each phy to indicate link activity and faults
- Provides an Inter-IC (I^2C) interface for enclosure management

Flexibility

These features increase the flexibility of the LSISAS1064:

- Supports a Flash ROM interface, an NVSRAM interface, and a pipelined synchronous burst SRAM (PSBRAM) interface
- Offers a flexible programming interface to tune I/O performance

- Allows mixed connections to SAS or SATA targets
- Leverages compatible connectors for SAS and SATA connections
- Allows grouping of up to four phys to form a wide port
- Allows programming of the World Wide Name

Reliability

These features enhance the reliability of the LSISAS1064:

- Uses proven GigaBlaze® transceivers
- Isolates the power and ground of I/O pads and internal chip logic
- Provides 2 kV ESD protection
- Provides latch-up protection
- Has a high proportion of power and ground pins
- Integrated RAID solution provides Integrated Mirroring technology and Integrated Striping technology
- Supports ZCR

Testability

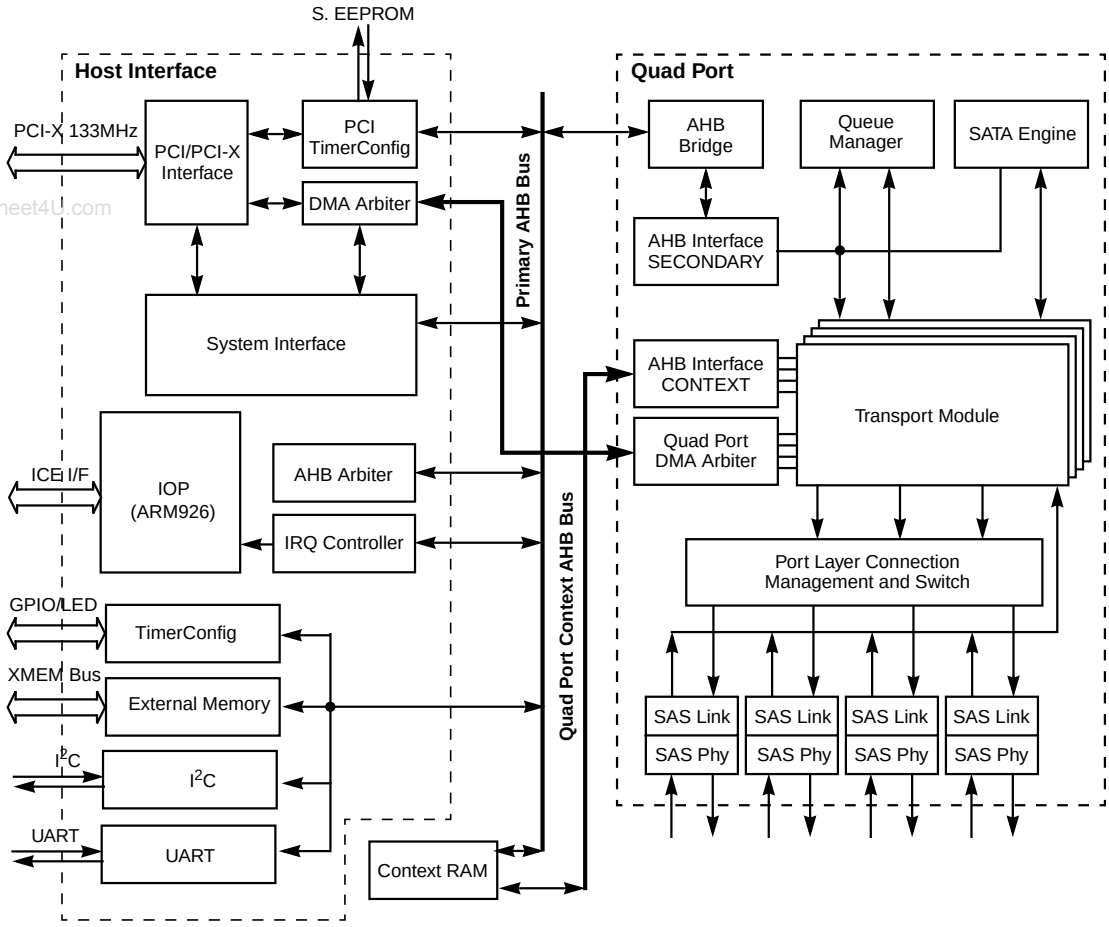
These features enhance the testability of the LSISAS1064:

- Offers JTAG boundary scan
- Provides a UART interface for debugging
- Offers ARM Multi-ICE® for debugging the ARM9 processor
- Offers I^2C port to output debug information

Block Diagram Description

Figure 3 provides the block diagram for the LSISAS1064 controller. The following subsections discuss the block diagram.

Figure 3 LSISAS1064 Controller Block Diagram



Host Interface

The LSISAS1064 interfaces with the host through the host interface module. The host interface module contains the PCI/PCI-X interface, system interface, PCI timer and configuration, DMA arbiter, IOP, I^2C, and external memory blocks.

PCI/PCI-X Interface

The LSISAS1064 provides a PCI-X interface that supports up to a 64-bit, 133 MHz PCI-X bus. With the exception that the PCI interface is not tolerant of 5 V PCI, the interface is backward compatible with all previous implementations of the PCI specification.

System Interface

In combination with the IOP, the system interface supports the Fusion-MPT architecture. The system interface efficiently passes messages between the LSISAS1064 and the host interface using a high-performance, packetized mailbox architecture. The LSISAS1064 system interface coalesces PCI interrupts to minimize traffic on the PCI bus and maximize system performance.

IOP

The LSISAS1064 I/O processor controls the system interface and manages the host side of the Fusion-MPT architecture without host processor intervention, which frees the host processor for other tasks.

Timer and Configuration

This block supports the LSISAS1064 LED and GPIO interfaces. The GPIO interface contains four independent GPIO signals. This block also supports internal timing adjustments and power-on sense configuration options.

DMA Arbiter

The LSISAS1064 provides the ability to transfer system memory blocks to and from local memory through the descriptor-based DMA arbiter and router. The DMA channel includes PCI bus master interface logic, a system DMA FIFO, and the internal bus interface logic.

PCI Timer and Configuration

This PCI timer and configuration module supports the PCI configuration register space, an industry-standard, 2-wire serial EEPROM interface, and a power-on reset (POR). A serial EEPROM is not required for typical system configurations.

External Memory

The external memory controller block provides an interface for Flash ROM, NVSRAM, and PSBRAM devices. The external memory bus provides a 32-bit memory bus, parity checking, and chip select signals for PSBRAM, NVSRAM, and Flash ROM. The Flash ROM and NVSRAM are capable of 8-bit accesses, while the PSBRAM is capable of 32-bit accesses.

Typical system configurations require a Flash ROM to store firmware, configuration information, and persistent data information.

Inter-IC (I^2C)

The LSISAS1064 contains an I^2C that communicates with peripherals, such as an enclosure management processor. This interface is also referred to as the Industry-Standard 2-Wire Interface (ISTWI). The I^2C block operates as either a master or a slave on the bus and sustains data rates up to 400 Kbits/s. The I^2C block accomplishes byte-wise bidirectional data transfers by using either an interrupt or a polling handshake at the completion of each byte. The style and operation of this interface closely follows the defacto standard for a two-wire serial interface chip. The I^2C block controls all bus timing and performs bus-specific sequences.

UART

The UART provides test and debug access to the LSISAS1064.

Quad Port

The quad port module in the LSISAS1064 implements the SSP, SMP, and STP/SATA protocols, and manages the four SAS/SATA phys. The following subsections describe the quad port module.

Transport Module

The transport modules transmit frames to and from the port layer and implement the STP, SSP, and SMP protocols. There are four instances of the transport module, one for each SAS/SATA phy on the LSISAS1064. The transport modules also manage DMA transfers.

Queue Manager

The queue manager is responsible for managing various queue structures that support the SSP, SMP, and SATA/STP protocols. The queue structures are the primary means for the IOP to initiate I/Os to the hardware and for the hardware to notify the IOP of I/O status.

SATA Engine

The SATA engine provides information to the transport modules to enable handling of SATA commands. The SATA engine tracks queued commands per device and provides these tags to the SATA transport layer blocks.

Port Layer Connection Manager and Switch

The port layer connection monitor and switch manages transmission requests from the transport modules and originates connection requests to the SAS links. It is also responsible for handling SAS wide port configurations.

SAS Link

The SAS link layer manages SAS connections between initiator and target ports, data clocking, and CRC checking on transmitted data. The SAS link is also responsible for starting a link reset sequence.

SAS Phy

The SAS phys interface to the physical layer, perform serial-to-parallel conversion of received data and parallel-to-serial conversion of transmit data, manage phy reset sequences, and perform 8b/10b encoding.

Quad Port Arbiter

The quad port arbiter interfaces with the host interface DMA arbiter and determines bus priority between each of the four ports for DMA transfers.

Context RAM

The context RAM is a memory that is shared between the host interface module and the quad port module. The context RAM holds a portion of the firmware.

Signal Description

The following subsections provide the signal descriptions for the LSISAS1064. A "/" following the signal indicates an active LOW signal.

PCI Signals

This section describes the PCI signals. Refer to the PCI specification for signal descriptions.

PCI System Signals

This section describes the PCI system signals.

CLK	**PCI Clock**	**Input**
RST/	**Reset**	**Input**

PCI Address and Data Signals

This section describes the PCI address and data signals.

AD[63:0]	**64-bit Address/Data bus**	**Input/Output**
C_BE[7:0]/	**Command/Byte Enable**	**Input/Output**
PAR	**Parity**	**Input/Output**
PAR64	**64-bit Parity**	**Input/Output**

PCI Interface Control Signals

This section describes the PCI interface control signals.

GNT/	**Grant**	**Input**
REQ/	**Request**	**Output**

REQ64/	**Request 64-bit**	**Input/Output**
ACK64/	**Acknowledge 64-bit**	**Input/Output**
IDSEL	**ID Select**	**Input**
FRAME/	**Frame**	**Input/Output**
IRDY/	**Initiator Ready**	**Input/Output**
TRDY/	**Target Ready**	**Input/Output**
DEVSEL/	**Device Select**	**Input/Output**
STOP/	**Stop**	**Input/Output**
PERR/	**Parity Error**	**Input/Output**
SERR/	**Error**	**Input/Output**
INTA/	**PCI Interrupt A**	**Output**

PCI-Related Signals

ALT_INTA/ **Alternate PCI Interrupt A** **Output**
The alternate interrupt signal is used for ZCR.

ALT_GNT/ **Read/Write Chip Select** **Input**
This active LOW signal provides a chip select during configuration read and write transactions. Enabling ZCR enables this signal.

ZCR_EN/ **Zero Channel RAID Enable** **Input**
This input configures the LSISAS1064 for ZCR operation. Deasserting this signal configures the LSISAS1064 for standard PCI/PCI-X operation. This signal is internally pulled HIGH.

BZR_SET **Reference Resistance** **Analog**
This signal provides the reference resistor node for the PCI-X impedance controller.

BZVDD **Reference Resistance** **Analog**
This signal provides the reference resistor node for the PCI-X impedance controller.

CompactPCI Signals

This section describes the CompactPCI signals.

CPCI_EN/ **CompactPCI Enable** **Input**
Enabling this active LOW signal configures the LSISAS1064 for the CompactPCI protocol. This signal is internally pulled HIGH.

CPCI_SWITCH
CompactPCI Switch **Input**
This active HIGH signal indicates to the LSISAS1064 device that a change in the system configuration is imminent. This signal is internally pulled LOW.

CPCI_ENUM/ **CompactPCI** **Input/Output**
This signal informs the system that a board either was freshly inserted or is about to be extracted. This signal remains asserted until the system driver services the hot-swapped board.

CPCI64_EN/ **CompactPCI 64-bit Enable** **Input**
This pin indicates the width of the PCI bus when CompactPCI is enabled. Designers must provide a pull-up on this pin when the device is enabled for CompactPCI operation. When CompactPCI is not enabled, designers must leave this pin unconnected.

CPCI_LED/ **CompactPCI LED** **Output**
This active LOW pin provides the CompactPCI Status LED. This is a 3.3 V output.

SAS Signals

This section describes the SAS interface signals.

REFCLK_P, REFCLK_N **Input**
These pins provide the serial differential clock. Connect a 75 MHz oscillator with an accuracy of at least 50ppm to these pins. To use a single-ended crystal, tie the crystal to REFCLK_P and tie REFCLK_N to a resistor termination.

RTRIM **Resistor Reference** **Analog**
This pin provides the analog resistor reference for the GigaBlaze transceivers.

RX[3:0]– **Receive Negative Differential Data** **Input**
RX[x]– provides the negative differential data receiver for phy[x].

RX[3:0]+ **Receive Positive Differential Data** **Input**
RX[x]+ provides the positive differential data receiver for phy[x].

TX[3:0]– **Transmit Negative Differential Data** **Output**
TX[x]– provides the negative differential data transmit signal for phy[x].

TX[3:0]+ **Transmit Positive Differential Data** **Output**
TX[x]+ provides the positive differential data transmit signal for each phy[x].

FAULT_LED[3:0]/
Fault LED **Output**
These output signals indicate a SAS link fault.

ACTIVE_LED[3:0]/
Activity LED **Output**
These output signals indicate SAS link activity.

I²C and Serial EEPROM Signals

This section describes the serial EEPROM and I²C signals.

SERIAL_CLK **Serial Interface Clock** **Input/Output**
This pin provides the serial EEPROM clock signal.

SERIAL_DATA
Serial Interface Data **Input/Output**
This pin provides the serial EEPROM data signal.

ISTW_CLK **I²C Clock** **Input/Output**
This pin provides the I²C clock signal.

ISTW_DATA **I²C Data** **Input/Output**
This pin provides the I²C data signal.

Memory Interface Signals

This section describes the memory interface pins.

MCLK **Memory Clock** **Output**
All synchronous RAM control/data signals reference the rising edge of this clock.

ADSC/ **Address-Strobe-Controller** **Output**
Asserting this active LOW signal initiates read, write, or chip deselect cycles.

ADV/ **Advance** **Output**
Asserting this active LOW signal increments the burst address counter of the selected synchronous SRAM.

MAD[31:0] **Multiplexed Address/Data** **Input/Output**
These signals provide the address and data bus to the PSBRAM, Flash ROM, and NVSRAM. These signals also provide Power-On Sense configuration functions to the LSISAS1064. These signals are internally pulled LOW.

MADP[3:0] **Memory Parity** **Input/Output**
These signals provide parity checking for MAD[31:0].

MOE[1:0]/ **Memory Output Enables** **Output**
Asserting these active LOW signals enable the selected PSBRAM, Flash ROM, or NVSRAM device to drive data. MOE[1]/ enables PSBRAM and Flash ROM devices. MOE[0]/ enables NVSRAM devices. MOE[1:0]/ allows interleaved PSBRAM configurations.

MWE[1:0]/ **Memory Write Enables** **Output**
The LSISAS1064 uses these active LOW bank write signals for interleaved PSBRAM configurations.

BWE[3:0]/ **Memory Byte Write Enables** **Output**
Asserting these active LOW, byte-lane write signals enable partial word writes to the PSBRAM. BWE[3]/ and BWE[2]/ enable partial word writes to the Flash ROM and the NVSRAM if FLASH_CS/ or NVSRAM_CS/ are asserted.

NVSRAM_CS/
NVSRAM Chip Select **Output**
Asserting this active LOW signal selects the NVSRAM device.

PSBRAM_CS/

RAM Chip Select **Output**

Asserting this active LOW signal selects the PSBRAMs. Up to four PSBRAMS are possible in an interleaved and depth-expanded configuration.

FLASH_CS/ **Flash Chip Select** **Output**

Asserting the active LOW signal selects the Flash ROM. The LSISAS1064 maps Flash ROM address space into system memory space.

Configuration and General Purpose Signals

This section describes the configuration and general purpose pins.

TST_RST/ **Test Reset** **Input**

Asserting this signal forces the chip into a Power-On-Reset state. This signal has an internal pull-up.

REFCLK_B **ARM Reference Clock** **Input**

This pin provides the ARM reference clock.

MODE[5:0] **Mode Select** **Input**

This bus defines operational and test modes for the chip. These pins have internal pull-downs.

GPIO[3:0] **General Purpose I/O** **Input/Output**

These pins provide general purpose input/output signals. These pins have internal pull-ups.

HB_LED/ **Heartbeat LED** **Output**

Firmware intermittently asserts this signal to indicate that the IOP is operational.

JTAG and Test Signals

This section describes the test and JTAG signals.

ECC[5:2] **ECC**

These signals are for LSI Logic test purposes only.

FSELA **Clock Select** **Input**

This is a test signal. Pull this signal LOW.

TCK **JTAG Debug Clock** **Input**

TRST/ **JTAG Debug Reset** **Input**

TDI	**JTAG Debug Test Data In**	**Input**
TDO	**JTAG Debug Test Data Out**	**Output**
TMS	**JTAG Debug Test Mode Select**	**Input**
TCK_ICE	**Multi-ICE Debug Clock**	**Input**
RTCK_ICE	**Multi-ICE Debug Return Clock**	**Output**
TRST_ICE/	**Multi-ICE Debug Reset**	**Input**
TDI_ICE	**Multi-ICE Debug Test Data In**	**Input**
TDO_ICE	**Multi-ICE Debug Test Data Out**	**Output**
TMS_ICE	**Multi-ICE Debug Test Mode Select**	**Input**
IDDTN	**IDDQ Test Mode Enable**	**Input**
TN/	**3-State Output Enable Control**	**Input**
PROCMON	**Process Monitor Test Output Driver**	**Output**
TMUXSPARE[7:0]	**Test Mux Spare**	**Input/Output**
TDIODE_P	**Anode Connection of the Thermal Diode**	**Input**
TDIODE_N	**Cathode Connection of the Thermal Diode**	**Output**

Power Signals and No Connects

This section describes the power and ground signals.

REFPLL_VDD **Power**

These signals provide 1.2 V power.

REFPLL_VSS **Ground**

These signals provide ground.

PLL_VDD **Power**

These signals provide 1.2 V power.

PLL_VSS **Ground**

These signals provide ground.

VDD2 **Power**

These signals provide 1.2 V core power.

VDDIO33 **Power**

These signals provide 3.3 V I/O power.

VDDIO5PCIX **Power**

These signals provide the bias reference for PCI pads.

VDDIO33PCIX **Power**

These signals provide 3.3 V PCI I/O power.

VSS2 **Ground**

These signals provide ground.

RX_VSS[3:0], RXB_VSS[3:0], TX_VSS[3:0], TXB_VSS[3:0] **Ground**

These signals provide ground for the GigaBlaze core.

RX_VDD[3:0], RXB_VDD[3:0], TX_VDD[3:0], TXB_VDD[3:0] **Power**

These signals provide 1.2 V power for the GigaBlaze core.

NC **No Connect**

No connect signals do not connect to the silicon inside of the LSISAS1064 package.

RESERVED

Reserved signals are reserved for LSI Logic use. These signals connect to the LSISAS1064 silicon. Do not connect to Reserved signals.

Pinout

Table 1 provides the signal listing by signal name. Table 2 provides the BGA pin listing. Figure 4 provides a BGA diagram.

Table 1 Listing by Signal Name

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ACK64/	AE18	AD[55]	AD23	MAD[3]	C25	N/C	D15
ACTIVE_LED[0]/	H4	AD[56]	AF22	MAD[4]	C24	N/C	D16
ACTIVE_LED[1]/	G1	AD[57]	AF23	MAD[5]	E24	N/C	D22
ACTIVE_LED[2]/	H1	AD[58]	AE22	MAD[6]	D26	N/C	E7
ACTIVE_LED[3]/	L5	AD[59]	AE23	MAD[7]	D24	N/C	E8
AD[0]	AF14	AD[60]	AF21	MAD[8]	D25	N/C	E9
AD[1]	AE17	AD[61]	AC19	MAD[9]	E25	N/C	E10
AD[2]	AD14	AD[62]	AF20	MAD[10]	C26	N/C	E15
AD[3]	AF15	AD[63]	AF19	MAD[11]	D23	N/C	E16
AD[4]	AF13	ADSC/	P23	MAD[12]	H21	N/C	E17
AD[5]	AF16	ADV/	U26	MAD[13]	H23	N/C	F9
AD[6]	AF12	ALT_GNT/	T5	MAD[14]	K24	N/C	G4
AD[7]	AE11	ALT_INTA/	U3	MAD[15]	H24	N/C	G6
AD[8]	AF10	BWE[0]/	N22	MAD[16]	V26	N/C	G22
AD[9]	AF11	BWE[1]/	M26	MAD[17]	T26	N/C	H5
AD[10]	AE9	BWE[2]/	J25	MAD[18]	T24	N/C	H6
AD[11]	AB12	BWE[3]/	N25	MAD[19]	R26	N/C	H22
AD[12]	AB10	BZR_SET	V21	MAD[20]	U25	N/C	J4
AD[13]	AF9	BZVDD	AA24	MAD[21]	R23	N/C	J6
AD[14]	AD10	C_BE[0]/	AE10	MAD[22]	Y26	N/C	J21
AD[15]	AF5	C_BE[1]/	AC8	MAD[23]	T22	N/C	J23
AD[16]	AF4	C_BE[2]/	AD6	MAD[24]	U24	N/C	K5
AD[17]	AE5	C_BE[3]/	AD2	MAD[25]	AA26	N/C	K22
AD[18]	AD4	C_BE[4]/	AF18	MAD[26]	V25	N/C	K25
AD[19]	AE4	C_BE[5]/	AD19	MAD[27]	V24	N/C	L22
AD[20]	Y6	C_BE[6]/	AF17	MAD[28]	W26	N/C	M4
AD[21]	Y8	C_BE[7]/	AE19	MAD[29]	R22	N/C	N4
AD[22]	AB3	CLK	Y4	MAD[30]	AA25	N/C	N5
AD[23]	AE3	CPCI64_EN/	U2	MAD[31]	AB26	N/C	N23
AD[24]	Y7	CPCI_LED/	M5	MADP[0]	G21	N/C	N24
AD[25]	AA5	CPCI_EN/	R1	MADP[1]	J26	N/C	P3
AD[26]	AA4	CPCI_ENUM/	U1	MADP[2]	P26	N/C	P4
AD[27]	AE1	CPCI_SWITCH	P1	MADP[3]	W23	N/C	P22
AD[28]	AB2	DEVSEL/	AD5	MCLK	N26	N/C	R4
AD[29]	AC1	ECC2	Y1	MODE[0]	F3	N/C	R5
AD[30]	V5	ECC3	V4	MODE[1]	E2	N/C	T25
AD[31]	AD1	ECC4	W3	MODE[2]	E3	N/C	U22
AD[32]	AB24	ECC5	U5	MODE[3]	D1	N/C	V6
AD[33]	AC26	FAULT_LED[0]/	F2	MODE[4]	F4	N/C	V22
AD[34]	AD26	FAULT_LED[1]/	E1	MODE[5]	C2	N/C	V23
AD[35]	AA23	FAULT_LED[2]/	J5	MOE[0]/	M22	N/C	W4
AD[36]	Y22	FAULT_LED[3]/	F1	MOE[1]/	E26	N/C	W6
AD[37]	W20	FLASH_CS/	H26	MWE[0]/	L26	N/C	W21
AD[38]	AB25	FRAME/	AB7	MWE[1]/	H25	N/C	W22
AD[39]	AC25	FSELA	G5	N/C	A11	N/C	Y5
AD[40]	AC24	GNT/	AA1	N/C	A16	N/C	Y21
AD[41]	Y20	GPIO[0]	J2	N/C	A21	N/C	AA7
AD[42]	AD24	GPIO[1]	K3	N/C	B8	N/C	AA8
AD[43]	AF25	GPIO[2]	L3	N/C	B22	N/C	AA18
AD[44]	AB21	GPIO[3]	K2	N/C	B23	N/C	AB8
AD[45]	AC20	HB_LED/	J3	N/C	C8	N/C	AB9
AD[46]	AA20	IDDTN	N1	N/C	C14	N/C	AB11
AD[47]	AD25	IDSEL	AD3	N/C	C15	N/C	AB13
AD[48]	AC23	INTA/	V3	N/C	C19	N/C	AB15
AD[49]	AA19	IRDY/	AF6	N/C	C20	N/C	AB16
AD[50]	AE25	ISTW_CLK	F22	N/C	D6	N/C	AC7
AD[51]	AE24	ISTW_DATA	F21	N/C	D7	N/C	AC9
AD[52]	AF24	MAD[0]	B26	N/C	D8	N/C	AC13
AD[53]	AB19	MAD[1]	F23	N/C	D9	N/C	AC14
AD[54]	AD22	MAD[2]	G23	N/C	D14	N/C	AC15

Note: *NC* pins are not connected to the LSISAS1064 silicon. RESERVED signals connect to the LSISAS1064 silicon. Do not connect to RESERVED signals.

Table 1 Listing by Signal Name (Cont.)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
N/C	AC18	TDI_ICE	F7	VDDIO33	C7	VSS2	B15
N/C	AC21	TDIODE_P	M23	VDDIO33	E4	VSS2	B19
N/C	AD11	TDIODE_N	K26	VDDIO33	E5	VSS2	B20
N/C	AE2	TDO	K1	VDDIO33	E22	VSS2	D5
N/C	AE14	TDO_ICE	B4	VDDIO33	F24	VSS2	D11
NVSRAM_CS/	G26	TMS	P2	VDDIO33	G3	VSS2	D17
PAR	AD9	TMS_ICE	A4	VDDIO33	G24	VSS2	E21
PAR64	AB17	TMUX_SPARE[0]	A3	VDDIO33	H3	VSS2	E23
PERR/	AF7	TMUX_SPARE[1]	A2	VDDIO33	K23	VSS2	F5
PLL_VDD	AC4	TMUX_SPARE[2]	E6	VDDIO33	L4	VSS2	F25
PLL_VSS	AC3	TMUX_SPARE[3]	C4	VDDIO33	L24	VSS2	G2
PROCMON	M1	TMUX_SPARE[4]	D4	VDDIO33	M3	VSS2	G8
PSBRAM_CS/	J24	TMUX_SPARE[5]	B3	VDDIO33	M24	VSS2	G25
REFCLK_B	D3	TMUX_SPARE[6]	C3	VDDIO33	N3	VSS2	H2
REFCLK_N	J22	TMUX_SPARE[7]	F6	VDDIO33	P24	VSS2	H20
REFCLK_P	F26	TN/	P5	VDDIO33	R3	VSS2	K4
REFPLL_VDD	D2	TRDY/	AA9	VDDIO33	R24	VSS2	L23
REFPLL_VSS	C1	TRST_ICE/	C5	VDDIO33	T3	VSS2	L25
REQ/	AB1	TRST/	L1	VDDIO33	T23	VSS2	M2
REQ64/	AD18	TST_RST/	G7	VDDIO33	U4	VSS2	M12
RESERVED	V2	TXB_VDD0	F19	VDDIO33PCIX	W24	VSS2	M14
RESERVED	W2	TXB_VDD1	E18	VDDIO33PCIX	Y3	VSS2	M25
RST/	W5	TXB_VDD2	A18	VDDIO33PCIX	Y24	VSS2	N2
RTCK_ICE	A5	TXB_VDD3	B10	VDDIO33PCIX	AA3	VSS2	N13
RTRIM	C9	TXB_VSS0	D21	VDDIO33PCIX	AB5	VSS2	N15
RXB_VDD0	G19	TXB_VSS1	D19	VDDIO33PCIX	AB22	VSS2	P12
RXB_VDD1	E19	TXB_VSS2	A17	VDDIO33PCIX	AB23	VSS2	P14
RXB_VDD2	C17	TXB_VSS3	C10	VDDIO33PCIX	AC5	VSS2	P25
RXB_VDD3	D12	TX0–	A23	VDDIO33PCIX	AC11	VSS2	R2
RXB_VSS0	G20	TX1–	A19	VDDIO33PCIX	AC17	VSS2	R13
RXB_VSS1	E20	TX2–	C13	VDDIO33PCIX	AD7	VSS2	R15
RXB_VSS2	B18	TX3–	A9	VDDIO33PCIX	AD8	VSS2	R25
RXB_VSS3	D13	TX0+	A24	VDDIO33PCIX	AD12	VSS2	T2
RX0–	B25	TX1+	A20	VDDIO33PCIX	AD13	VSS2	T4
RX1–	C21	TX2+	B13	VDDIO33PCIX	AD15	VSS2	U23
RX2–	C16	TX3+	A10	VDDIO33PCIX	AD16	VSS2	W7
RX3–	A14	TX_VDD0	C22	VDDIO33PCIX	AD20	VSS2	W25
RX0+	B24	TX_VDD1	C18	VDDIO33PCIX	AD21	VSS2	Y2
RX1+	B21	TX_VDD2	E13	VDDIO5PCIX	V1	VSS2	Y19
RX2+	B16	TX_VDD3	B9	VDDIO5PCIX	W1	VSS2	Y25
RX3+	A13	TX_VSS0	D20	VDDIO5PCIX	Y23	VSS2	AA2
RX_VDD0	C23	TX_VSS1	D18	VDDIO5PCIX	AA6	VSS2	AA22
RX_VDD1	A22	TX_VSS2	A15	VDDIO5PCIX	AA21	VSS2	AB4
RX_VDD2	E14	TX_VSS3	E11	VDDIO5PCIX	AB14	VSS2	AB6
RX_VDD3	A12	UART_RX	F8	VDDIO5PCIX	AB18	VSS2	AC10
RX_VSS0	F20	UART_TX	A6	VDDIO5PCIX	AB20	VSS2	AC16
RX_VSS1	F18	VDD2	C11	VDDIO5PCIX	AC2	VSS2	AC22
RX_VSS2	B17	VDD2	C12	VDDIO5PCIX	AC6	VSS2	AE7
RX_VSS3	E12	VDD2	D10	VDDIO5PCIX	AC12	VSS2	AE8
SCAN_ENABLE	B2	VDD2	M13	VDDIO5PCIX	AD17	VSS2	AE12
SCAN_MODE	H7	VDD2	M15	VDDIO5PCIX	AF8	VSS2	AE13
SERIAL_CLK	A8	VDD2	N12	VSS2	A25	VSS2	AE15
SERIAL_DATA	A7	VDD2	N14	VSS2	B1	VSS2	AE16
SERR/	AF3	VDD2	P13	VSS2	B6	VSS2	AE20
STOP/	AE6	VDD2	P15	VSS2	B7	VSS2	AE21
TCK	L2	VDD2	R12	VSS2	B11	VSS2	AE26
TCK_ICE	B5	VDD2	R14	VSS2	B12	VSS2	AF2
TDI	J1	VDDIO33	C6	VSS2	B14	ZCR_EN/	T1

Note: *NC* pins are not connected to the LSISAS1064 silicon. RESERVED signals connect to the LSISAS1064 silicon. Do not connect to RESERVED signals.

Table 2 Listing by Pin Number

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A2	TMUX_SPARE[1]	C12	VDD2	E21	VSS2	J22	REFCLK_N
A3	TMUX_SPARE[0]	C13	TX2–	E22	VDDIO33	J23	N/C
A4	TMS_ICE	C14	N/C	E23	VSS2	J24	PSBRAM_CS/
A5	RTCK_ICE	C15	N/C	E24	MAD[5]	J25	BWE[2]/
A6	UART_TX	C16	RX2–	E25	MAD[9]	J26	MADP[1]
A7	SERIAL_DATA	C17	RXB_VDD2	E26	MOE[1]/	K1	TDO
A8	SERIAL_CLK	C18	TX_VDD1	F1	FAULT_LED[3]/	K2	GPIO[3]
A9	TX3–	C19	N/C	F2	FAULT_LED[0]/	K3	GPIO[1]
A10	TX3+	C20	N/C	F3	MODE[0]	K4	VSS2
A11	N/C	C21	RX1–	F4	MODE[4]	K5	N/C
A12	RX_VDD3	C22	TX_VDD0	F5	VSS2	K22	N/C
A13	RX3+	C23	RX_VDD0	F6	TMUX_SPARE[7]	K23	VDDIO33
A14	RX3–	C24	MAD[4]	F7	TDI_ICE	K24	MAD[14]
A15	TX_VSS2	C25	MAD[3]	F8	UART_RX	K25	N/C
A16	N/C	C26	MAD[10]	F9	N/C	K26	TDIODE_N
A17	TXB_VSS2	D1	MODE[3]	F18	RX_VSS1	L1	TRST/
A18	TXB_VDD2	D2	REFPLL_VDD	F19	TXB_VDD0	L2	TCK
A19	TX1–	D3	REFCLK_B	F20	RX_VSS0	L3	GPIO[2]
A20	TX1+	D4	TMUX_SPARE[4]	F21	ISTW_DATA	L4	VDDIO33
A21	N/C	D5	VSS2	F22	ISTW_CLK	L5	ACTIVE_LED[3]/
A22	RX_VDD1	D6	N/C	F23	MAD[1]	L22	N/C
A23	TX0–	D7	N/C	F24	VDDIO33	L23	VSS2
A24	TX0+	D8	N/C	F25	VSS2	L24	VDDIO33
A25	VSS2	D9	N/C	F26	REFCLK_P	L25	VSS2
B1	VSS2	D10	VDD2	G1	ACTIVE_LED[1]/	L26	MWE[0]/
B2	SCAN_ENABLE	D11	VSS2	G2	VSS2	M1	PROCMON
B3	TMUX_SPARE[5]	D12	RXB_VDD3	G3	VDDIO33	M2	VSS2
B4	TDO_ICE	D13	RXB_VSS3	G4	N/C	M3	VDDIO33
B5	TCK_ICE	D14	N/C	G5	FSELA	M4	N/C
B6	VSS2	D15	N/C	G6	N/C	M5	CPCI_LED/
B7	VSS2	D16	N/C	G7	TST_RST/	M12	VSS2
B8	N/C	D17	VSS2	G8	VSS2	M13	VDD2
B9	TX_VDD3	D18	TX_VSS1	G19	RXB_VDD0	M14	VSS2
B10	TXB_VDD3	D19	TXB_VSS1	G20	RXB_VSS0	M15	VDD2
B11	VSS2	D20	TX_VSS0	G21	MADP[0]	M22	MOE[0]/
B12	VSS2	D21	TXB_VSS0	G22	N/C	M23	TDIODE_P
B13	TX2+	D22	N/C	G23	MAD[2]	M24	VDDIO33
B14	VSS2	D23	MAD[11]	G24	VDDIO33	M25	VSS2
B15	VSS2	D24	MAD[7]	G25	VSS2	M26	BWE[1]/
B16	RX2+	D25	MAD[8]	G26	NVSRAM_CS/	N1	IDDTN
B17	RX_VSS2	D26	MAD[6]	H1	ACTIVE_LED[2]/	N2	VSS2
B18	RXB_VSS2	E1	FAULT_LED[1]/	H2	VSS2	N3	VDDIO33
B19	VSS2	E2	MODE[1]	H3	VDDIO33	N4	N/C
B20	VSS2	E3	MODE[2]	H4	ACTIVE_LED[0]/	N5	N/C
B21	RX1+	E4	VDDIO33	H5	N/C	N12	VDD2
B22	N/C	E5	VDDIO33	H6	N/C	N13	VSS2
B23	N/C	E6	TMUX_SPARE[2]	H7	SCAN_MODE	N14	VDD2
B24	RX0+	E7	N/C	H20	VSS2	N15	VSS2
B25	RX0–	E8	N/C	H21	MAD[12]	N22	BWE[0]/
B26	MAD[0]	E9	N/C	H22	N/C	N23	N/C
C1	REFPLL_VSS	E10	N/C	H23	MAD[13]	N24	N/C
C2	MODE[5]	E11	TX_VSS3	H24	MAD[15]	N25	BWE[3]/
C3	TMUX_SPARE[6]	E12	RX_VSS3	H25	MWE[1]/	N26	MCLK
C4	TMUX_SPARE[3]	E13	TX_VDD2	H26	FLASH_CS/	P1	CPCI_SWITCH
C5	TRST_ICE/	E14	RX_VDD2	J1	TDI	P2	TMS
C6	VDDIO33	E15	N/C	J2	GPIO[0]	P3	N/C
C7	VDDIO33	E16	N/C	J3	HB_LED/	P4	N/C
C8	N/C	E17	N/C	J4	N/C	P5	TN/
C9	RTRIM	E18	TXB_VDD1	J5	FAULT_LED[2]/	P12	VSS2
C10	TXB_VSS3	E19	RXB_VDD1	J6	N/C	P13	VDD2
C11	VDD2	E20	RXB_VSS1	J21	N/C	P14	VSS2

Note: *NC* pins are not connected to the LSISAS1064 silicon. RESERVED signals connect to the LSISAS1064 silicon. Do not connect to RESERVED signals.

Table 2 Listing by Pin Number (Cont.)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
P15	VDD2	W6	N/C	AB15	N/C	AD20	VDDIO33PCIX
P22	N/C	W7	VSS2	AB16	N/C	AD21	VDDIO33PCIX
P23	ADSC/	W20	AD[37]	AB17	PAR64	AD22	AD[54]
P24	VDDIO33	W21	N/C	AB18	VDDIO5PCIX	AD23	AD[55]
P25	VSS2	W22	N/C	AB19	AD[53]	AD24	AD[42]
P26	MADP[2]	W23	MADP[3]	AB20	VDDIO5PCIX	AD25	AD[47]
R1	CPCI_EN/	W24	VDDIO33PCIX	AB21	AD[44]	AD26	AD[34]
R2	VSS2	W25	VSS2	AB22	VDDIO33PCIX	AE1	AD[27]
R3	VDDIO33	W26	MAD[28]	AB23	VDDIO33PCIX	AE2	N/C
R4	N/C	Y1	ECC2	AB24	AD[32]	AE3	AD[23]
R5	N/C	Y2	VSS2	AB25	AD[38]	AE4	AD[19]
R12	VDD2	Y3	VDDIO33PCIX	AB26	MAD[31]	AE5	AD[17]
R13	VSS2	Y4	CLK	AC1	AD[29]	AE6	STOP/
R14	VDD2	Y5	N/C	AC2	VDDIO5PCIX	AE7	VSS2
R15	VSS2	Y6	AD[20]	AC3	PLL_VSS	AE8	VSS2
R22	MAD[29]	Y7	AD[24]	AC4	PLL_VDD	AE9	AD[10]
R23	MAD[21]	Y8	AD[21]	AC5	VDDIO33PCIX	AE10	C_BE[0]/
R24	VDDIO33	Y19	VSS2	AC6	VDDIO5PCIX	AE11	AD[7]
R25	VSS2	Y20	AD[41]	AC7	N/C	AE12	VSS2
R26	MAD[19]	Y21	N/C	AC8	C_BE[1]/	AE13	VSS2
T1	ZCR_EN/	Y22	AD[36]	AC9	N/C	AE14	N/C
T2	VSS2	Y23	VDDIO5PCIX	AC10	VSS2	AE15	VSS2
T3	VDDIO33	Y24	VDDIO33PCIX	AC11	VDDIO33PCIX	AE16	VSS2
T4	VSS2	Y25	VSS2	AC12	VDDIO5PCIX	AE17	AD[1]
T5	ALT_GNT/	Y26	MAD[22]	AC13	N/C	AE18	ACK64/
T22	MAD[23]	AA1	GNT/	AC14	N/C	AE19	C_BE[7]/
T23	VDDIO33	AA2	VSS2	AC15	N/C	AE20	VSS2
T24	MAD[18]	AA3	VDDIO33PCIX	AC16	VSS2	AE21	VSS2
T25	N/C	AA4	AD[26]	AC17	VDDIO33PCIX	AE22	AD[58]
T26	MAD[17]	AA5	AD[25]	AC18	N/C	AE23	AD[59]
U1	CPCI_ENUM/	AA6	VDDIO5PCIX	AC19	AD[61]	AE24	AD[51]
U2	CPCI64_EN/	AA7	N/C	AC20	AD[45]	AE25	AD[50]
U3	ALT_INTA/	AA8	N/C	AC21	N/C	AE26	VSS2
U4	VDDIO33	AA9	TRDY/	AC22	VSS2	AF2	VSS2
U5	ECC5	AA18	N/C	AC23	AD[48]	AF3	SERR/
U22	N/C	AA19	AD[49]	AC24	AD[40]	AF4	AD[16]
U23	VSS2	AA20	AD[46]	AC25	AD[39]	AF5	AD[15]
U24	MAD[24]	AA21	VDDIO5PCIX	AC26	AD[33]	AF6	IRDY/
U25	MAD[20]	AA22	VSS2	AD1	AD[31]	AF7	PERR/
U26	ADV/	AA23	AD[35]	AD2	C_BE[3]/	AF8	VDDIO5PCIX
V1	VDDIO5PCIX	AA24	BZVDD	AD3	IDSEL	AF9	AD[13]
V2	RESERVED	AA25	MAD[30]	AD4	AD[18]	AF10	AD[8]
V3	INTA/	AA26	MAD[25]	AD5	DEVSEL/	AF11	AD[9]
V4	ECC3	AB1	REQ/	AD6	C_BE[2]/	AF12	AD[6]
V5	AD[30]	AB2	AD[28]	AD7	VDDIO33PCIX	AF13	AD[4]
V6	N/C	AB3	AD[22]	AD8	VDDIO33PCIX	AF14	AD[0]
V21	BZR_SET	AB4	VSS2	AD9	PAR	AF15	AD[3]
V22	N/C	AB5	VDDIO33PCIX	AD10	AD[14]	AF16	AD[5]
V23	N/C	AB6	VSS2	AD11	N/C	AF17	C_BE[6]/
V24	MAD[27]	AB7	FRAME/	AD12	VDDIO33PCIX	AF18	C_BE[4]/
V25	MAD[26]	AB8	N/C	AD13	VDDIO33PCIX	AF19	AD[63]
V26	MAD[16]	AB9	N/C	AD14	AD[2]	AF20	AD[62]
W1	VDDIO5PCIX	AB10	AD[12]	AD15	VDDIO33PCIX	AF21	AD[60]
W2	RESERVED	AB11	N/C	AD16	VDDIO33PCIX	AF22	AD[56]
W3	ECC4	AB12	AD[11]	AD17	VDDIO5PCIX	AF23	AD[57]
W4	N/C	AB13	N/C	AD18	REQ64/	AF24	AD[52]
W5	RST/	AB14	VDDIO5PCIX	AD19	C_BE[5]/	AF25	AD[43]

Note: *NC* pins are not connected to the LSISAS1064 silicon. RESERVED signals connect to the LSISAS1064 silicon. Do not connect to RESERVED signals.

Figure 4 LSISAS1064 472-Pin BGA Top View

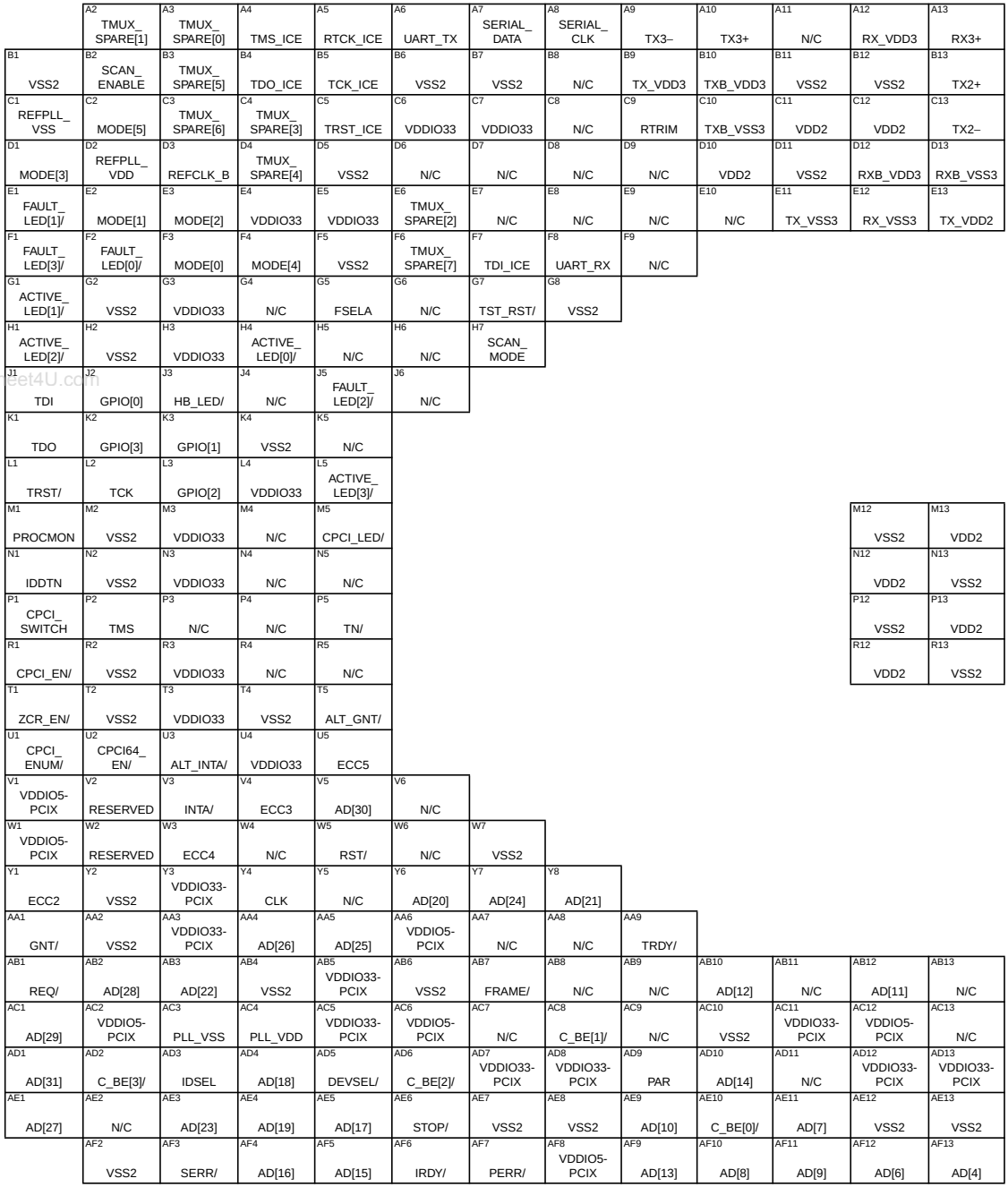
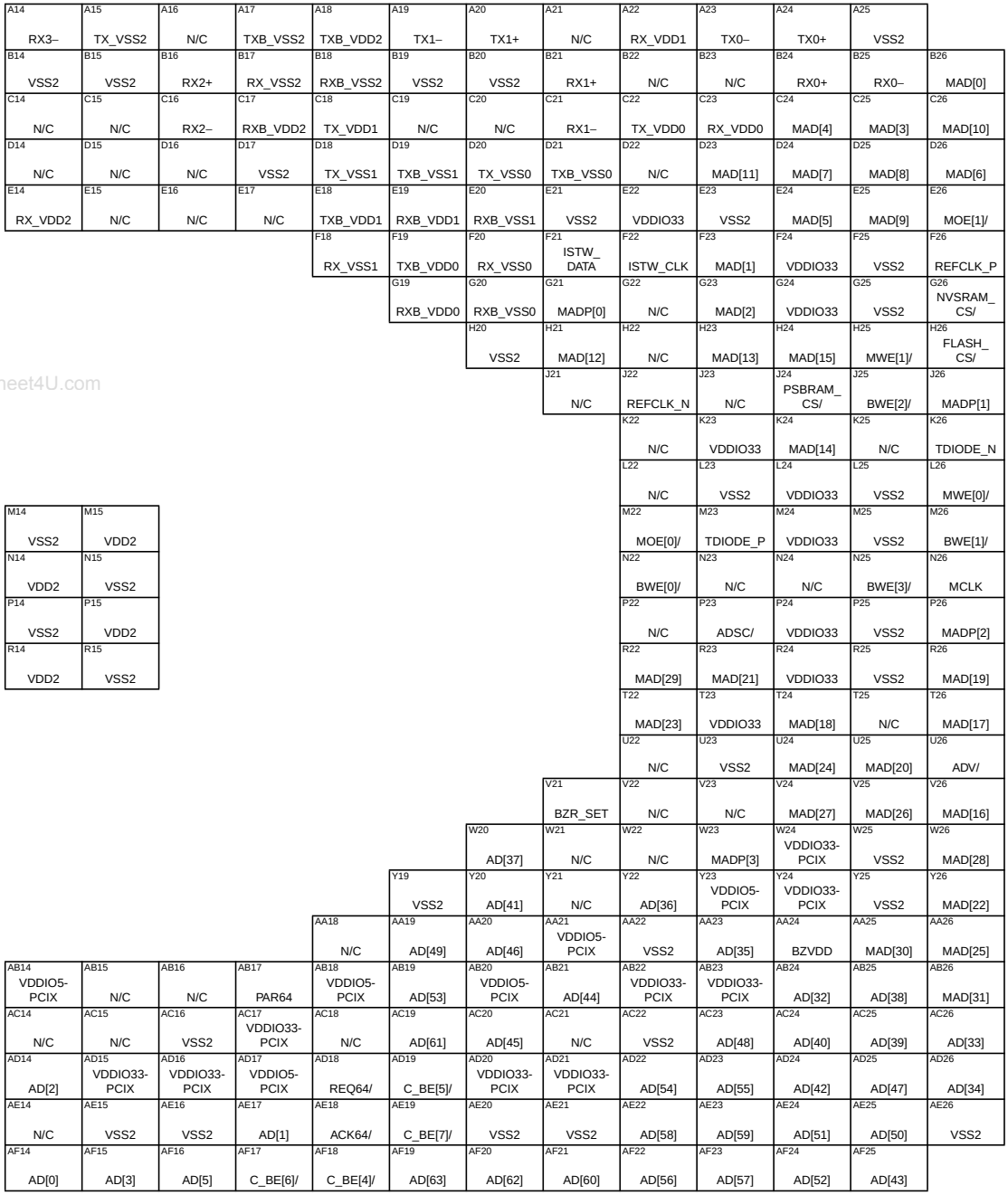


Figure 4 LSISAS1064 472-Pin BGA Top View (Cont.)



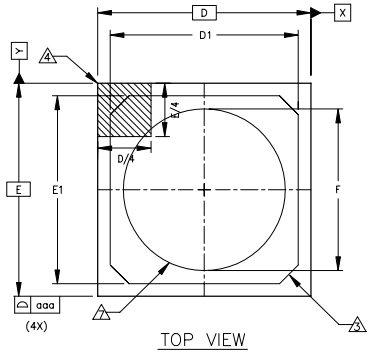
A14 RX3–	A15 TX_VSS2	A16 N/C	A17 TXB_VSS2	A18 TXB_VDD2	A19 TX1–	A20 TX1+	A21 N/C	A22 RX_VDD1	A23 TX0–	A24 TX0+	A25 VSS2	
B14 VSS2	B15 VSS2	B16 RX2+	B17 RX_VSS2	B18 RXB_VSS2	B19 VSS2	B20 VSS2	B21 RX1+	B22 N/C	B23 N/C	B24 RX0+	B25 RX0–	B26 MAD[0]
C14 N/C	C15 N/C	C16 RX2–	C17 RXB_VDD2	C18 TX_VDD1	C19 N/C	C20 N/C	C21 RX1–	C22 TX_VDD0	C23 RX_VDD0	C24 MAD[4]	C25 MAD[3]	C26 MAD[10]
D14 N/C	D15 N/C	D16 N/C	D17 VSS2	D18 TX_VSS1	D19 TXB_VSS1	D20 TX_VSS0	D21 TXB_VSS0	D22 N/C	D23 MAD[11]	D24 MAD[7]	D25 MAD[8]	D26 MAD[6]
E14 RX_VDD2	E15 N/C	E16 N/C	E17 N/C	E18 TXB_VDD1	E19 RXB_VDD1	E20 RXB_VSS1	E21 VSS2	E22 VDDIO33	E23 VSS2	E24 MAD[5]	E25 MAD[9]	E26 MOE[1]/
				F18 RX_VSS1	F19 TXB_VDD0	F20 RX_VSS0	F21 ISTW_ DATA	F22 ISTW_CLK	F23 MAD[1]	F24 VDDIO33	F25 VSS2	F26 REFCLK_P
					G19 RXB_VDD0	G20 RXB_VSS0	G21 MADP[0]	G22 N/C	G23 MAD[2]	G24 VDDIO33	G25 VSS2	G26 NVSRAM_ CS/
						H20 VSS2	H21 MAD[12]	H22 N/C	H23 MAD[13]	H24 MAD[15]	H25 MWE[1]/	H26 FLASH_ CS/
							J21 N/C	J22 REFCLK_N	J23 N/C	J24 PSBRAM_ CS/	J25 BWE[2]/	J26 MADP[1]
								K22 N/C	K23 VDDIO33	K24 MAD[14]	K25 N/C	K26 TDIODE_N
								L22 N/C	L23 VSS2	L24 VDDIO33	L25 VSS2	L26 MWE[0]/
M14 VSS2	M15 VDD2							M22 MOE[0]/	M23 TDIODE_P	M24 VDDIO33	M25 VSS2	M26 BWE[1]/
N14 VDD2	N15 VSS2							N22 BWE[0]/	N23 N/C	N24 N/C	N25 BWE[3]/	N26 MCLK
P14 VSS2	P15 VDD2							P22 N/C	P23 ADSC/	P24 VDDIO33	P25 VSS2	P26 MADP[2]
R14 VDD2	R15 VSS2							R22 MAD[29]	R23 MAD[21]	R24 VDDIO33	R25 VSS2	R26 MAD[19]
								T22 MAD[23]	T23 VDDIO33	T24 MAD[18]	T25 N/C	T26 MAD[17]
								U22 N/C	U23 VSS2	U24 MAD[24]	U25 MAD[20]	U26 ADV/
							V21 BZR_SET	V22 N/C	V23 N/C	V24 MAD[27]	V25 MAD[26]	V26 MAD[16]
						W20 AD[37]	W21 N/C	W22 N/C	W23 MADP[3]	W24 VDDIO33-PCIX	W25 VSS2	W26 MAD[28]
					Y19 VSS2	Y20 AD[41]	Y21 N/C	Y22 AD[36]	Y23 VDDIO5-PCIX	Y24 VDDIO33-PCIX	Y25 VSS2	Y26 MAD[22]
				AA18 N/C	AA19 AD[49]	AA20 AD[46]	AA21 VDDIO5-PCIX	AA22 VSS2	AA23 AD[35]	AA24 BZVDD	AA25 MAD[30]	AA26 MAD[25]
AB14 VDDIO5-PCIX	AB15 N/C	AB16 N/C	AB17 PAR64	AB18 VDDIO5-PCIX	AB19 AD[53]	AB20 VDDIO5-PCIX	AB21 AD[44]	AB22 VDDIO33-PCIX	AB23 VDDIO33-PCIX	AB24 AD[32]	AB25 AD[38]	AB26 MAD[31]
AC14 N/C	AC15 N/C	AC16 VSS2	AC17 VDDIO33-PCIX	AC18 N/C	AC19 AD[61]	AC20 AD[45]	AC21 N/C	AC22 VSS2	AC23 AD[48]	AC24 AD[40]	AC25 AD[39]	AC26 AD[33]
AD14 AD[2]	AD15 VDDIO33-PCIX	AD16 VDDIO33-PCIX	AD17 VDDIO5-PCIX	AD18 REQ64/	AD19 C_BE[5]/	AD20 VDDIO33-PCIX	AD21 VDDIO33-PCIX	AD22 AD[54]	AD23 AD[55]	AD24 AD[42]	AD25 AD[47]	AD26 AD[34]
AE14 N/C	AE15 VSS2	AE16 VSS2	AE17 AD[1]	AE18 ACK64/	AE19 C_BE[7]/	AE20 VSS2	AE21 VSS2	AE22 AD[58]	AE23 AD[59]	AE24 AD[51]	AE25 AD[50]	AE26 VSS2
AF14 AD[0]	AF15 AD[3]	AF16 AD[5]	AF17 C_BE[6]/	AF18 C_BE[4]/	AF19 AD[63]	AF20 AD[62]	AF21 AD[60]	AF22 AD[56]	AF23 AD[57]	AF24 AD[52]	AF25 AD[43]	

Package Drawings

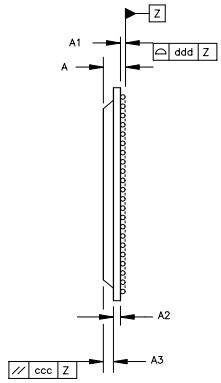
The LSISAS1064 is packaged in a 472-EPBGA-T package with a 27 mm x 27 mm footprint and 1.0 mm ball pitch. The package code is UO. The package drawing number is JZ02-000015-00. Figure 5 provides the package diagram for the LSISAS1064.

Figure 5 472-Pin EPBGA-T (UO) Mechanical Drawing

REVISIONS			
APPROVAL	DATE	DESCRIPTION	REV
C.FISHLEY	01-24-02	INITIAL RELEASE	0
C.FISHLEY	03-20-02	REVISE DIMENSION (ddd)	1
R.MENDOZA	01-29-03	ADD PACKAGE (4E)	2
C.FISHLEY	06-04-03	ADD PACKAGE (6i)	3
C.FISHLEY	06-25-03	ADD PACKAGE (61)	4
WK Liew	10-06-03	ADD PACKAGE (4X) (5E) (HT)	5
L. MORA	03-24-04	ADD PACKAGE (5Y)	6
WK Liew	07-02-04	ADD PACKAGE (8C)	7
C. Fishley	08-13-04	ADD PACKAGE (uo, 3w, ow, 82)	8



TOP VIEW



SIDE VIEW

TABLE 1: COMMON DIMENSIONS			
SYM	MIN	NOM	MAX
A	–	–	2.50
A1	0.40	–	–
A2	0.25	–	0.70
A3	–	–	1.25
b	0.50	–	0.70
D		27.00 BSC	
D1	23.00	–	25.00
E		27.00 BSC	
E1	23.00	–	25.00
e		1.00 BSC	
F	19.50	–	21.50

TABLE 2: TOLERANCES OF FORM AND POSITION	
DIMENSION	e = 1.00
aaa	0.20
ccc	0.35
ddd	0.15
eee	0.25
fff	0.10

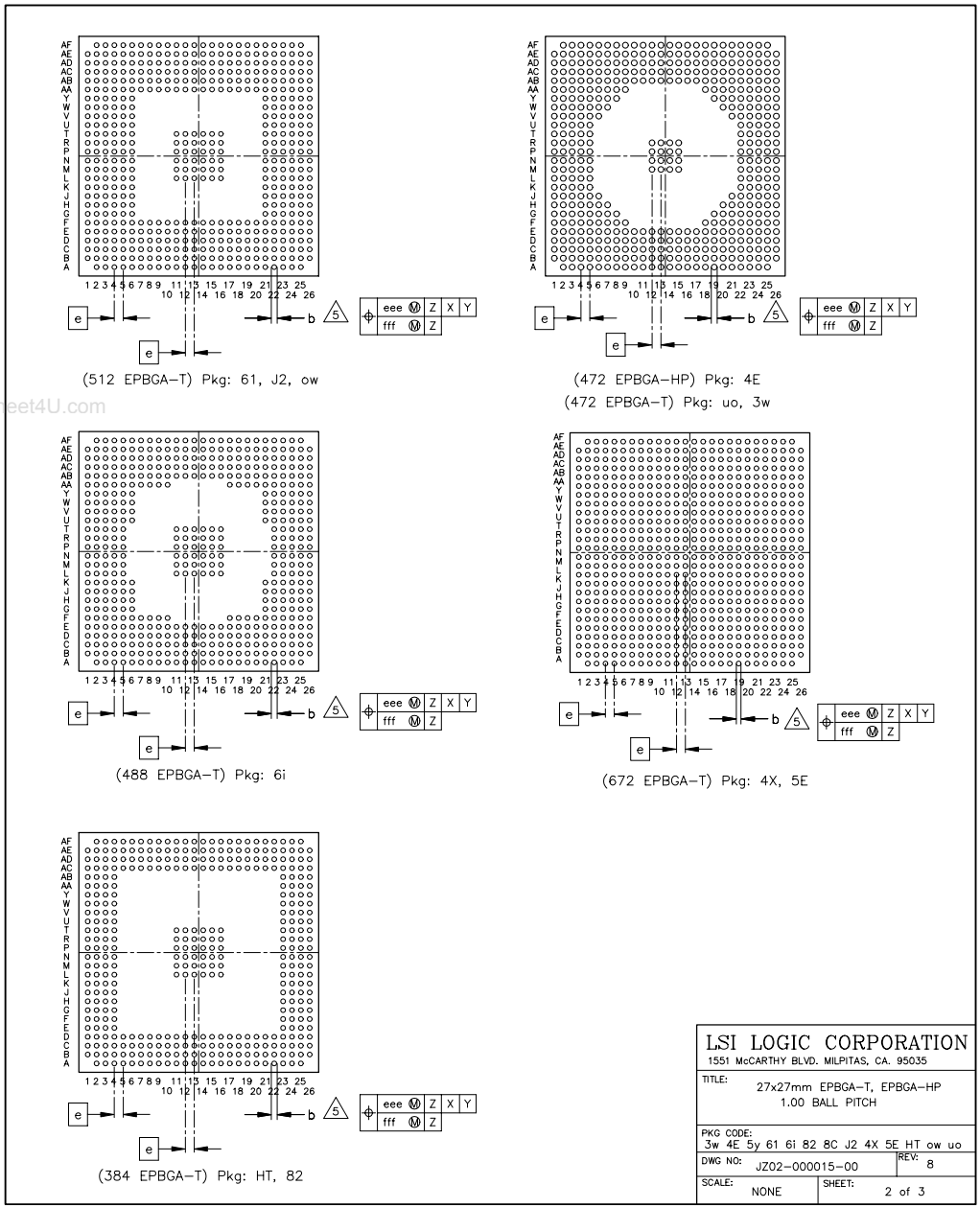
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS IN MM.
3. CORNER DETAIL IS LSI LOGIC CORPORATION OPTION.
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, AND MAY CONSIST OF INK, LASER MARK OR METALLIZED MARKING, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
5. JEDEC CODE MS–034.
6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. HEAT SPREADER OUTLINE.

LSI LOGIC CORPORATION 1551 McCARTHY BLVD. MILPITAS, CA. 95035	
TITLE:	27x27mm EPBGA–T, EPBGA–HP 1.00 BALL PITCH
PKG CODE:	3w 4E 5y 61 6i 82 8C J2 4X 5E HT ow uo
DWG NO: JZ02–000015–00	REV: 8
SCALE: NONE	SHEET: 1 of 3

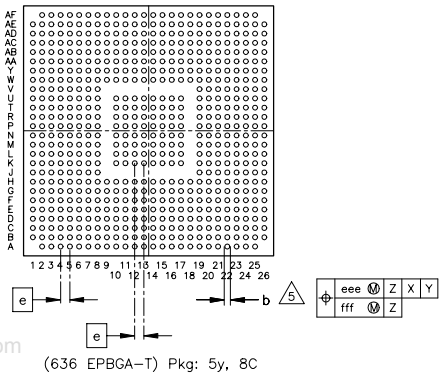
Important: **For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UO.**

Figure 5 472-Pin EPBGA-T (UO) Mechanical Drawing—Bottom View (Cont.)



Important: **For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UO.**

Figure 5 472-Pin EPBGA-T (UO) Mechanical Drawing—Bottom View (Cont.)



LSI LOGIC CORPORATION	
1551 McCARTHY BLVD. MILPITAS, CA. 95035	
TITLE:	27x27mm EPBGA–T, EPBGA–HP 1.00 BALL PITCH
PKG CODE:	3w 4E 5y 61 6i 82 8C J2 4X 5E HT ow uo
DWG NO: JZ02–000015–00	REV: 8
SCALE: NONE	SHEET: 3 of 3

Important: **For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UO.**

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